In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the new mandatory amendment format. Please amend claims 13, 15 and 16. Please add new claims 18-20.

1. (Previously Presented) A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time event at the personal computer indicating a request to process the real time data;

determining whether the real-time event has a higher priority than a first non-real time event being processed at the personal computer; and

processing the real-time data if the real-time event has a higher priority than the first non-real time event.

2. (Previously Presented) The method of claim 1 further comprising continuing to process the first non-real time event if the real-time event does not have a higher priority than the first event.

3. (Previously Presented) The method of claim 1 further comprising:

saving the state of the first non-real time event at the personal computer prior to processing the real-time event; and

processing the first non-real time event after processing of the real-time event has been completed.

4. (Previously Presented) The method of claim 1 further comprising:

receiving a second non-real time event while processing the real-time event; and

determining whether the second non-real time event has a higher priority than the real-time event.

5. (Previously Presented) The method of claim 4 further comprising:

continuing the processing of the real-time event if the second non-real time event does not have a higher priority than the real time event.

6. (Previously Presented) The method of claim 4 further comprising:

terminating the processing of the real-time event if the second non-real time event has a higher priority; and

processing the second non-real time event.

7. (Previously Presented) A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), coupled to the bus, to generate a real-time event upon receiving real-time analog data at the computer system and to process the real-time event if the real-time event has a higher priority than a non-real-time event.

8. (Previously Presented) The computer system of claim 7 wherein the CPU comprises:

a timer to generate timing signals at predetermined time intervals; and

an event mechanism coupled to the timer to generate the real time events.

9. (Previously Presented) The computer system of claim 8 wherein the CPU further comprises an event handler coupled to the event mechanism to process the real-time events.

10. (Original) The computer system of claim 9 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data.

11. (Previously Presented) The computer system of claim 9 wherein the event mechanism determines the relative priority between the real-time events and the non-real-time events.

12. (Original) The computer system of claim 11 wherein the CPU further comprises an analog to digital converter coupled to the register.

13. (Currently Amended) A central processing unit (CPU) comprising:

a timer to generate timing signals at predetermined time intervals;

a register coupled to the event mechanism to store real-time data received at the CPU as analog data;

an event mechanism coupled to the timer and the register to generate real time events in response to receiving the timing signals and determining that real-time data is stored within the register; and

an event handler coupled to the event mechanism to process the real-time events received from the event mechanism upon determining the relative priority between the real-time events and non-real-time events.

14. (Currently Amended) The ~~computer system~~ CPU of claim 13 wherein the ~~CPU further comprises a register coupled to the event mechanism to store real-time data~~ real-time analog data is data received from an analog radio coupled to the CPU.

15. (Currently Amended) The ~~computer system~~ CPU of claim ~~14~~ 13 wherein the event handler verifies whether there is data stored in register upon detecting a real-time event and determines the priority of the real-time event relative to other interrupts received.

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16. (Currently Amended) The ~~computer system~~ CPU of claim ~~14~~ 13 wherein the CPU further comprises an analog to digital converter coupled to the register to convert the real-time analog data to digital data.

17. (Previously Presented) The method of claim 1 wherein receiving the real-time analog data comprises:

converting the real-time analog data to digital data; and

storing the digital data at a register.

18. (New) The method of claim 17 wherein generating the real-time event comprises:

receiving a timing signal at an event mechanism at a predetermined interval;

the event mechanism determining whether data is stored within the register; and

generating the real-time event if data is stored within the register

19. (New) The computer system of claim 10 wherein the event mechanism generates the real time events in response to receiving the timing signals from the timer and determining that real-time data is stored within the register.

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20. (New) The computer system of claim 7 wherein the real-time analog data is data received from an analog radio.